

Remarks

In view of the above amendments and the following remarks, reconsideration of the rejections and further examination are requested.

Claims 1-4 have been rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 3 and 7 of U.S. Patent No. 6,661,469. Enclosed herewith is a Terminal Disclaimer linking the present application to U.S. Patent No. 6,661,469. As a result, withdrawal of this rejection is respectfully requested.

Claims 1-4 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Shigeta (US 6,064,456).

Claims 1-4 have been amended so as to further distinguish the present invention from the reference relied upon in the rejection. As a result, the rejection is submitted to be inapplicable to the claims for the following reasons.

Claim 1 is patentable over Shigeta, since claim 1 recites a false contour correcting apparatus having, in part, a double bit change detection circuit for detecting a signal portion in a digital image signal where a difference between a pixel value of a first pixel and a pixel value of a second pixel adjacent to the first pixel is two pixel value units, and outputting a signal representing results of the detection as a double bit change detection signal. Shigeta fails to disclose or suggest the double bit change detection circuit of claim 1.

Shigeta discloses a false contour correcting circuit 3 for correcting a false contour of pixel data D in a plasma display system. The circuit 3 includes a high-figure bit change detecting circuit 31, a selector control circuit 36, a delay circuit 32, first, second and third data converting circuits 33-35, and a selector 37. (See column 5, lines 16-21 and Figure 3).

In the rejection, the bit change detecting circuit 31 is relied upon as corresponding to the claimed double bit change detection circuit. The bit change detecting circuit 31 includes three circuits 310a-310c for respectively comparing the three most significant bits of the pixel data D of a pixel Z with the three most significant bits of pixel data of a pixel adjacent to the pixel Z. More specifically, if the most significant bit of the pixel data D of the pixel Z has the same value as the most significant bit of the pixel data of the adjacent pixel, the circuit 310a outputs a signal P1 having a logic value of "0". Otherwise, if the values of the most significant bits are different, the circuit 310a outputs the signal P1 having a logic value of "1". The circuits 310b and 310c operate in the same manner as the circuit 310a, but perform their comparisons on the second and

third most significant bits and output signals P2 and P3, respectively. Further, the bit change detecting circuit 31 includes an OR gate OR2 that performs an OR operation on the signals P1-P3 and outputs a signal P. (See column 5, line 27 – column 6, line 21 and Figure 4).

Based on the discussion of the bit change detecting circuit 31, it is clear that the bit change detecting circuit 31 ignores the fourth-sixth most significant bits of the pixel data D of the pixel Z when performing the comparison with the adjacent pixel. Therefore, for example, if the pixel data D of the pixel Z has a pixel value of “101000” and the pixel data of the pixel adjacent to the pixel Z has a pixel value of “101010”, the bit change detecting circuit 31 of Shigeta will not detect any difference between the pixel values of the two pixels, even though the pixel value of the adjacent pixel has increased by two pixel value units as compared the pixel value of the pixel Z (i.e., a change from “101000” to “101001” is a change of one pixel value unit, and a change from “101001” to “101010” is a second change of one pixel value unit). On the other hand, the double bit change detection circuit recited in claim 1 will detect this difference. Specifically, claim 1 recites that the double bit change detection circuit detects a signal portion in a digital image signal where a difference between a pixel value of a first pixel and a pixel value of a second pixel adjacent to the first pixel is two pixel value units.

In light of the above explanation, it is clear that the bit change detecting circuit 31 of Shigeta does not correspond to the claimed double bit change detection circuit. Further, since the purpose of the bit change detecting circuit 31 is obviously different than that of the claimed double bit change detection circuit based on the differences in operation, it clearly would not have been obvious to one of ordinary skill in the art to modify the bit change detecting circuit 31 to operate in a manner similar to the claimed double bit change detection circuit. As a result, claim 1 is patentable over Shigeta.

Additionally, it is noted that the rejection of claim 1-4 as being unpatentable over Shigeta is incomplete. The rejection admits that Shigeta fails to disclose a change in graduation, but fails to provide any explanation as to why the limitation is obvious. Instead, this portion of the rejection includes an incomplete sentence where the explanation should be located. (See page 6, “However, Shigeta”).

As for claim 3, it is patentable over Shigeta for reasons similar to those set forth above in support of claim 1. That is, claim 3 recites, in part, a double bit change detecting operation of detecting a signal portion in a digital image signal where a difference between a pixel value of a

first pixel and a pixel value of a second pixel adjacent to the first pixel is two pixel value units, which feature is not disclosed or suggested by the reference.

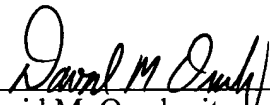
Because of the above-mentioned distinctions, it is believed clear that claims 1-4 are patentable over the reference relied upon in the rejection. Furthermore, it is submitted that the distinctions are such that a person having ordinary skill in the art at the time of invention would not have been motivated to make any combination of the references of record in such a manner as to result in, or otherwise render obvious, the present invention as recited in claims 1-4. Therefore, it is submitted that claims 1-4 are clearly allowable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. The Examiner is invited to contact the undersigned by telephone if it is felt that there are issues remaining which must be resolved before allowance of the application.

Respectfully submitted,

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